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A Study of Different Types of Voltage & Current Sense Amplifiers used in SRAM

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Abstract: The paper aims to study different types of voltage and current sense amplifiers which are used to read SRAM memory data. The review discusses the working operation, advantages, and disadvantages of various sense amplifiers. Method to decide feature size of different transistors in sense amplifiers has also been discussed. The paper focuses on various performance parameters which should be considered during designing of sense amplifiers.

Keywords: CMOS, SRAM, CTSA, Bit lines, Pre-charge circuit.

I INTRODUCTION

Performance of embedded memory and its peripheral circuits can adversely affect the speed and power of overall system. Sense Amplifier is the most vital circuits in the periphery of CMOS memory as its function is to sense or detect stored data from read selected memory.

The performance of sense amplifiers strongly affects both memory access time and overall memory power dissipation. The fallouts of increased memory capacity are increased bit line capacitance which in turn makes memory slower and more energy hungry. A sense amplifier is an active circuit that reduces the time of signal propagation from an accessed memory cell to the logic circuit located at the periphery of the memory cell array and converts thearbitrary logic levels occurring on a bit line to the digital logic levels of the peripheral Boolean circuits.

To improve the speed, performance of memory and to provide signals which confirm the requirements of driving peripheral circuits within the memory, understanding and analyzing the circuit design of different sense amplifier types and other substantial elements of sense circuits is necessary. This paper is divided into 5 sections. Section 1 provides the introduction of sense amplifier while section 2 & section 3 describes different types of sense amplifiers. Section 4 describes different parameters that should be considered during designing of sense amplifier & section 5 presents the conclusion of this paper.

II LITERATURE SURVEY OF VARIOUS SENSE AMPLIFIERS

On the basis of operation modes, a sense amplifier may be classified as:

1. Voltage Sense Amplifier
2. Current Sense Amplifier
3. Charge Transfer Sense Amplifier (CTSA)

The simplest voltage sense amplifier is the differential couple. When a cell is being read, a small voltage swing appears on the bit line which is further amplified by differential couple and use to drive digital logic. However the bit line voltage swing is becoming smaller and is reaching the same magnitude as bit line noise, the voltage sense amplifier become unusable.

The fundamental reason for applying current mode sense amplifier in sense circuit is their small input impedances. Benefits of small input and output impedances are reductions in sense circuit delays, voltage swings, cross-talking, substrate currents and substrate voltage modulations.

The operation of the CTSA is based on the charge re distribution mechanism between very high bit line capacitance and low output capacitance of the sense amplifier. A differential charge transfer amplifier takes advantage of the increased bit-line capacitance and also offers a low-power operation without sacrificing the speed.

III VOLTAGE SENSE AMPLIFIER

The voltage sense amplifier can be classified as follows:

A. Basic Differential Voltage Sense amplifier
B. Positive feedback differential voltage sense **a**mplifier
C. Latch type voltage sense amplifier

A. Basic Differential Voltage Sense Amplifier

The basic MOS differential voltage sense amplifier circuit contains all elements required for differential sensing. A differential amplifier takes small signal differential inputs and amplifies them to a large signal single ended output. The effectiveness of a differential amplifier is characterized by its ability to reject common noise and amplify true difference between the signals. Because of rather slow operational speed provided at considerable power dissipation and inherently high offset basic differential voltage amplifier is not applied in memories.

The basic differential voltage sense amplifier is shown in Figure, it contains of two NMOS transistors M1 and M2 and three resistors R1, R2 and R3. This circuit amplifies the small difference at bit lines to full swing at output nodes.

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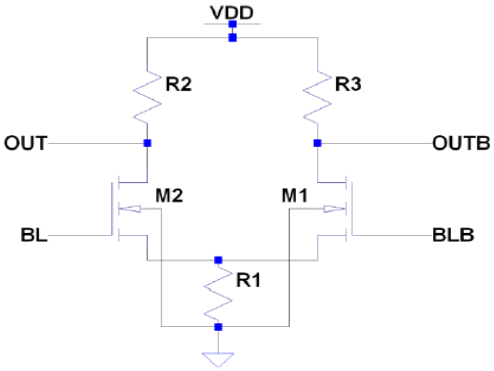

Fig.1. Differential Voltage Sense Amplifier

B. Positive Feedback Differential Voltage Sense Amplifier

Positive feedback sense amplifier is shown in below Figure 2, it comprises M1-M4 transistors as positive feedback amplifier and M5 , M6 are used to enable the sense amplifier, M7 is used to pre-charge the output node during pre-charge mode. The positive feedback amplifier has two data nodes BL/OUT and BLB/OUTB and three control nodes SEN, SEP and PRE. Nodes BL/OUT and BLB/OUTB act as both input and output to the sense amplifier. Its operation is as follows, the data nodes are equalized using PRE and the memory cell being read is asserted and a small voltage difference forms on BL/OUT and BLB/OUTB, while M1 and M2 are biased to be operating in the saturation region. M6 is turned on by SEN. As both BL/OUT and BLB/OUTB are decreasing in voltage so is the difference between them and one of them decreases much faster than the other and causes M1 orM2 to enter cut off while the other starts operating in triode, at this point M5 is turned on by SEP which pulls the signals rapidly apart. At this point since BL/OUT and BLB/OUTB, are directly connected to the bit-lines the data is automatically written to the destructively read memory cell. Due to its positive feedback this voltage sensing amplifier achieves a very high differential gain. This high gain minimizes sensing time by being able to sense small voltage swings on the bit line.

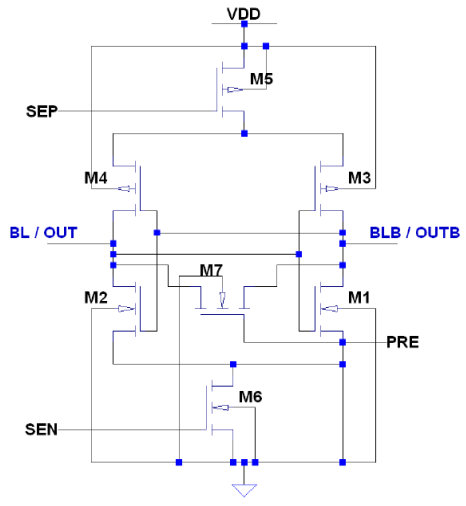

Fig.2. Positive Feedback Differential voltage sense amplifier

IV. Current sense amplifier

Current sense amplifier can be broadly classified as:
A. Current mirror sense amplifier
B. Current latched sense amplifier

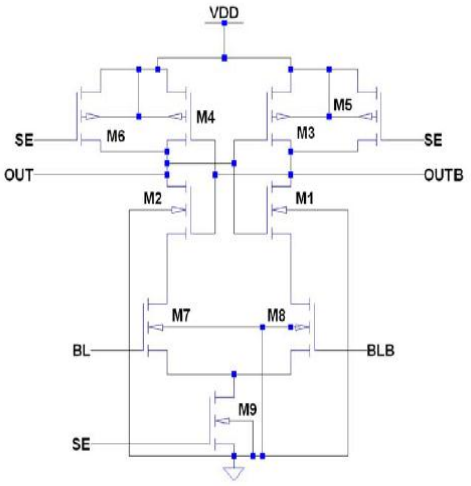

Fig.3. Latch type Voltage Sense Amplifier

C. *Latch Type Voltage Sense Amplifier*

The latch-type sense amplifier shown in Figure 3 , it comprises M1- M4 transistor as high gain positive feedback amplifier and M5 And M6 are used to pre-charge the output node and M9 is used to enable the sense amplifier, M7 and M8 are act as common source differential amplifier. Latch type sense amplifier is commonly used due to its advantages of low power dissipation and high speed.

C. Advanced current latched sense amplifier
D. High Speed low power latch type sense amplifier

A. Current Mirror Sense Amplifier

The traditional form of the primitive current amplifier is the current mirror amplifier. In the current-mirror amplifier, if devices M1 and M2 are identical, then the bit line or input current Ii is the same as the read line or output current Io , because the gate-source voltage Vgs is common for both devices.

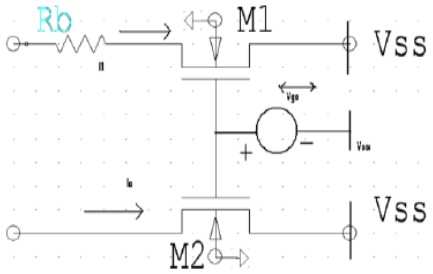

Fig.4. Current Mirroring and Multiplication

The conventional current-mirror sense amplifier in figure 5 is easy to control with the sense-amplifier activation timing signal, SE, and the speed of the current-mirror

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sense amplifier can be easily accelerated by increasing the operating current. Thus, memories frequently use this type of sense amplifier. However, the static current flows through the transistor MNS connected to ground; to accelerate the sense speed needs much power.

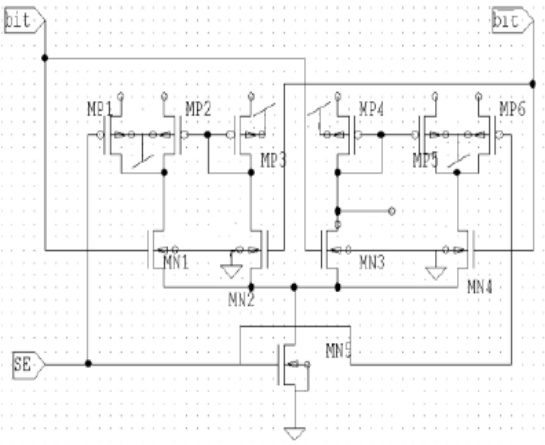

Fig.5.Current Mirror Sense Amplifier

B. Current Latched Sense Amplifier

The Current Latched Sense Amplifier (CLSA) is shown in Figure 6 . The bit line signal difference affects on the gate voltage of transistors MN1 and MN2, and the drains of transistors MP1, MN5, MP2 and MN4 are output nodes. There is no current flow from bit lines to output nodes. When sensing signal SE is at logic 0 (GND), the output node is isolated to GND, and the pre-charge transistors MP3, MP4 charge output nodes to Vdd.

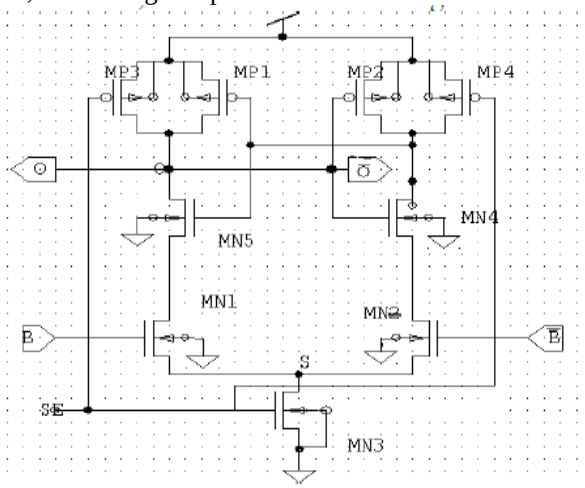

Fig. 6.Current Latched Sense Amplifier

When the sensing signal SE changes to logic 1 (Vdd), MN3 is turned on and the node S is pulled down to GND level. Under this condition, MN1 and MN2 are working as a common source differential amplifier. The voltage difference between B and B bar is transferred to the output nodes O and O bar by the common source differential amplifier. After a small voltage difference between O and O bar is generated, the cross-coupled amplifier which is constructed by MN4, MN5, MP1 and MP2 will finally amplify the voltage difference between O and O to a full swing voltage level. Therefore, we can sense and amplify the bit line signal without any current drifting from bit line to output node. This result shows that the bit line voltages will not be amplified, so the sensing and pre-charging power dissipation will be reduced. However, the CLSA has four transistors cascaded from Vdd to GND. This is a major disadvantage of CLSA to work at low working voltage (under 1.8v). When CLSA is working at low voltage, the differential current may be too small to be used for fast operation, which would even lead to the erroneous operation. Advantage of using this sense amplifier is reduction in sensing and pre-charging power dissipation.

C. Advanced Current Latched Sense Amplifier

A high-speed sense amplifier using the switch circuits (MN5, MN6, MP7 and MP8) to improve the power consumption and operation speed. Figure 7 illustrates the circuit architecture. Notably, the input node bit (bit bar) is controlled by the sensing signal and is isolated to the output node out bar (out). Thus the sensing power can be reduced. Also, a better performance at lower working voltage can be obtained by using the switch circuits. Two operation modes, the precharge mode and the sense mode, are analyzed and discussed as follows:

1. Pre-charge Mode:

In the pre-charge mode, the sensing signal SE is at logic 0 and the output nodes out bar (out) must be cleared for preparing the next sensing operation. Restated, the transistors MP7 and MP8 of the switch circuit are turned off in this mode. Thus, the input signals from bit lines cannot enter the sense amplifier and the drain voltages of transistors MN5 and MN6 are pulled down to zero. At this condition, transistors MNl, M N2, MN3 and MN4 are turned off and the output nodes out bar *(out)* can be charged to Vdd through the pre-charge transistors MP1 and MP6**.** Notably, the output nodes will hold at Vdd level since transistors MN1 and MN4 are turned off.

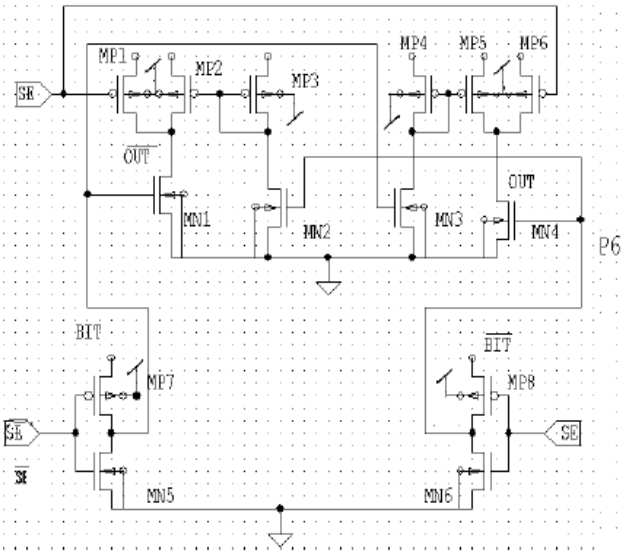

Fig.7. Advanced Current Latched Sense Amplifier

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The sensing signal SE is set at logic 1 in the sense mode operation. In this mode, the transistors MP7 and MP8 of the switch circuit are turned on, meanwhile transistors MN5 and MN6 are turned off. Thus, the input signals bits (bit bar) are transferred to the sense amplifier and transistors MN1, MN4 can work as a common source differential amplifier. Restated, a drain-to-source current difference between transistors MN1 and MN4 are induced. Finally, the current mirror architecture constructed by transistors MP2, MP3, MP4 and MP5 will convert and amplify the current difference to a voltage difference between the output nodes out bar and out. Advantage of this sense amplifier is reduced sensing delay . It can operate quite well at supply voltage from 1.8-3.3 V. Thus, applying such circuits in VLSI design can improve the performance and reduce the power consumption. This design is more complicated than any other current sense amplifier circuits.

D. High speed low power latch type sense amplifier:

This SA is shown in Figure 8 .There are only three transistor stages cascaded from VDD to GND. Note that the transistor stage number is less than that of lower working voltage can be obtained. CLSA, and the input nodes B, B are isolated to output nodes O, O bar. It is expected that the proposed SA has the same power consumption as CLSA; meanwhile a better performance at lower working voltage can be obtained. The circuit operation is described as follows. In Pre-charge Mode, the sensing signal SE is at logic 0. In this mode, the data on output nodes must be cleared and the SA prepares for next sensing operation. Because the sensing signals SE=0 and SE bar =1, MP1, MP4, MN5 and MN6 turn on, meanwhile MP5, MP6 turn off. Thus the input signals from bit lines can't enter through MP5 and MP6. Nodes 1 and 2 are pulled down to GND

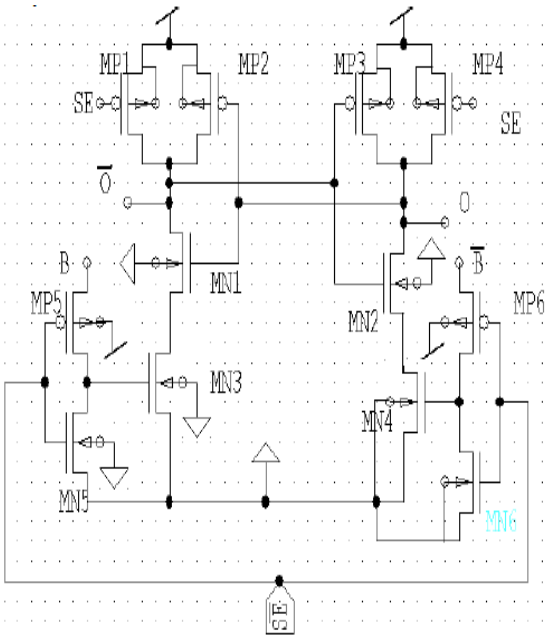

Fig.8. High speed low power Latch Type Sense Amplifier

level by MN5, MN6, so MN3, and MN4 will be cut off. The pre-charge transistors MP1, MP4 charge the output nodes to Vdd. Because MN3, MN4 are turned off, both the output nodes will hold at Vdd level. In this time interval, the operation detail is shown in Figure 9.

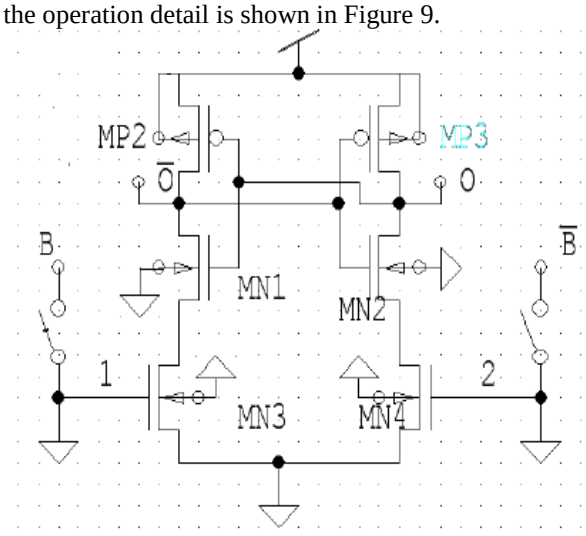

Fig.9. Sense Amplifier in Pre-charge mode

In Sense Mode, the sensing signal SE is at logic 1. In this mode, the bit line input signals B, and B bar must be transferred to SA's differential input nodes 1 and 2. Therefore, MN3 and MN4 work as a common source differential amplifier. This operation situation is just like CLSA in sensing operation. As the sensing signals SE=1 and SE bar =0, MP5, MP6 turn on and MN5, MN6, MP1, MP4 turn off. The bit line signals are transferred to nodes 1 and 2 by MP5 and MP6.The voltage difference between nodes 1 and 2 induces a drain-to-source current difference between MN3 and MN4. Finally, the cross-coupled amplifier constructed by MP2, MP3, MN1 and MN2 will convert and amplify the current difference to a voltage difference between output nodes O, and O bar. For a very short time, the full swing logic value appears on output nodes. This operation detail is shown in Figure 10.

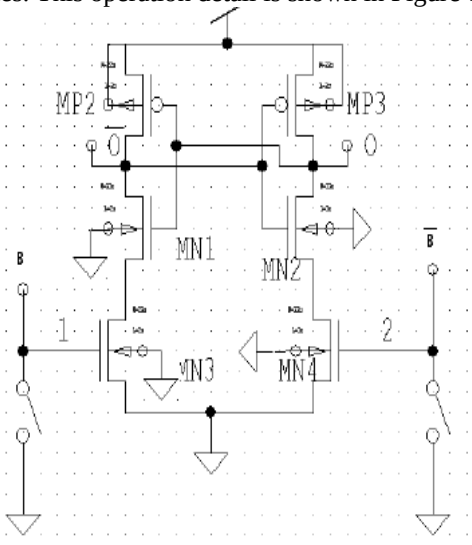

Fig.10. Sense Amplifier in Sense Mode

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This sense amplifier which is implemented in CMOS process can work at voltage as low as 1V. This design has 14% and 63% power delay product improvement over the advanced current latch SA and conventional sense amplifier, respectively. Disadvantage of this circuit design is that due to process variations, current mismatch in the evaluation branches of the sense amplifier circuit, resulting in operational failures and other drawback of this sense amplifier is its large size.

IV. Designing Sense Amplifier

Following are the performance metrics to be considered during the design of sense amplifier:

1. Minimum sensing delay,
2. Maximum voltage swing,
3. Minimum power consumption,
4. Optimized layout area,
5. High reliability,
6. Specified environmental tolerance.

Sense amplifier comprises mainly three part access transistor, driver transistor and load transistor Figure 11 shows the schematic of basic cell structure sense amplifier it consists of six transistors where MN5 and MN6 is called the access transistor and MN3 and MN4 is called the driver transistor and MP3 and MP4 called the load transistor.

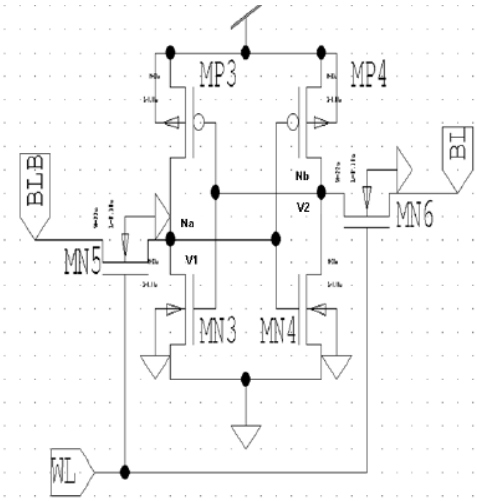

Fig.11.Basic cell when "0" is stored

To understand the working of basic cell we have to assume the previous state of cell. Suppose cell has already store the high data that will result out the node Na has high status and node Nb has the low status, that results out the transistor MP4 & MN3 gets on and MP3 & MN4 gets off. When the data comes to the bit lines of the cell, suppose zero is being placed on the bit line and one is placed on the bit complement line. As soon as the word line goes to high then node Na will discharge through the bit lines and will goes to low status which forces the transistor MN4 to become off and when node Nb goes high it will force MN3 Transistor to gets on. In this way the cell will flip the state from MN3 and MP4 off to MN4 and MP3 gets on. In this way the write operation get performed and after the write operation word lines goes to low status when the word line goes to low the pass transistor gets off and data which is get stored in the cell remains as such as long as the power supply is apply.

A. To decide W/L for driver, access and load transistor of sense amplifier

After making a schematic we have to set the W/L ratio of the driver, access and load transistor which we have used in the basic cell design in any CMOS circuit design W/L ratio is important parameter because this is the only parameter in the hand of the design engineer. So it should be carefully selected in the design of memory cell.

There are number of design criteria must be taken into consideration. The two basic criteria which usually considered during designing:

1. The data read operation should not be destructive.
2. Static noise margin should be in the acceptable range.

We take the static noise margin (SNM) consideration to calculate the W/L ratio. SNM is defined as maximum value of noise that can be tolerated by cross coupled inverters before altering the state SNM is very important parameter to design any of the memory cell because it indicate the stability of the cell .
From the literature survey, we find that

W/L ratio of the load transistor = 2

W/L ratio of the access transistor = 2

W/L ratio of the driver transistor = 3

V. CONCLUSION

A comparative study of different types of voltage and current sense amplifiers has been carried out. From this study, we can conclude that out of voltage and current sense amplifier, later one is better. Among different current sense amplifiers , advanced current latched sense amplifier and high speed low power latch type current sense amplifier have minimum sensing delay and power consumption . These two sense amplifiers even operate at low voltage ranging from 1.8-3.3 V. Even high speed low power current sense amplifier can sense the lowest possible swing from SRAM bit lines with the fast response time as compare to other sense amplifiers.

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